AMENDMENTS TO THE CLAIMS

1. (Currently amended) A lateral transistor comprising:

a semiconductor substrate of ~~the~~ a first conductivity type;

a buried base region of ~~the~~ a second conductivity type opposite to the first conductivity type, disposed on said semiconductor substrate;

a uniform base region of the second conductivity type disposed on said first buried base region, the uniform base region having a uniform lateral doping profile, the lateral doping profile being measured along a lateral direction parallel to the top surface of said semiconductor substrate;

a plug region of the second conductivity type disposed in said uniform base region, the plug region protrudes from a top surface of said uniform base region so as to reach to said buried base region;

a first ~~and second~~ main electrode ~~regions~~ region of the first conductivity type disposed in and at the top surface of said uniform base region~~, the first and second main electrode regions being aligned in the lateral direction~~; ~~and~~

a graded base region of the second conductivity type disposed in said uniform base region, enclosing bottom and side of said first main electrode region such that said first main electrode region is disposed in the center at the top surface of the graded base region, ~~the graded base region having a doping profile such that impurity concentration decreases gradually along the lateral direction towards said second main electrode region from said first main electrode region,~~ and

a second main electrode region of the first conductivity type disposed in and at the top surface of said uniform base region so as to directly contact with said uniform base region, the second main electrode region being aligned in the lateral direction with the first main electrode region configured such that a main current of the lateral transistor flows along the lateral direction between the first and second main electrode regions,

wherein the graded base region has a doping profile such that impurity concentration decreases gradually along the lateral direction towards said second main electrode region from said first main electrode region, and when the lateral transistor is not biased

wherein a combination of said buried base region, said uniform base region and said graded base region serves as a base region.

2. (Previously presented) The lateral transistor of claim 1, wherein said second main electrode region is formed in a frame shape along the top surface of said uniform base region, configured such that said second main electrode region laterally surrounds said graded base region.

3. (Previously presented) The lateral transistor of claim 2, wherein said second main electrode region is formed in a rectangular frame shape.

4. (Original) The lateral transistor of claim 1, further comprising a base contact region disposed in and at a top surface of said plug region.

5. (Previously presented) The lateral transistor of claim 2, further comprising a base wiring being in contact with said base contact region.

6. (Currently amended) A semiconductor integrated circuit including a lateral transistor, the lateral transistor comprising:

a semiconductor substrate of ~~the~~ a first conductivity type;

a first buried region of ~~the~~ a second conductivity type opposite to the first conductivity type, disposed on said semiconductor substrate;

a uniform base region of the second conductivity type disposed on said first buried region, the uniform base region having a uniform lateral doping profile, the lateral doping profile being measured along a lateral direction parallel to the top surface of said semiconductor substrate;

a first plug region of the second conductivity type disposed in said uniform base region, the first plug region protrudes from a top surface of said uniform base region so as to reach to said first buried region;

a first ~~and second~~ main electrode ~~regions~~ region of the first conductivity type disposed in and at the top surface of said uniform base region~~, the first and second main electrode regions being aligned in the lateral direction~~; ~~and~~

a graded base region of the second conductivity type disposed in said uniform base region, enclosing bottom and side of said first main electrode region such that said first main electrode region is disposed in the center at the top surface of the graded base region, ~~the graded base region has a doping profile such that impurity concentration decreases gradually along the lateral direction towards said second main electrode region from said first main electrode region,~~

a second main electrode region of the first conductivity type disposed in and at the top surface of said uniform base region so as to directly contact with said uniform base region, the second main electrode region being aligned in the lateral direction with the first main electrode region configured such that a main current of the lateral transistor flows along the lateral direction between the first and second main electrode regions.

wherein the graded base region has a doping profile such that impurity concentration decreases gradually along the lateral direction towards said second main electrode region from said first main electrode region, and

wherein a combination of said first buried region, said uniform base region and said graded base region serves as a first base region of said lateral transistor.

7. (Currently amended) The semiconductor integrated circuit of claim 6, further including a vertical transistor, the vertical transistor comprising:

a second buried region of the second conductivity type disposed on said semiconductor substrate, the second buried region serving as a part of a third main electrode region of said vertical transistor;

a drift region of the second conductivity type disposed on said second buried region;

a second base region of the first conductivity type disposed in said drift region; and

a fourth main electrode region of the second conductivity type disposed in said second base region, configured such that a main current of the vertical transistor flows along a vertical direction to the top surface of said semiconductor substrate, the main current flows between the third and fourth main electrode regions.

8. (Previously presented) The semiconductor integrated circuit of claim 7, further comprising a connecting wiring configured to connect said second main electrode region and second base region.

9. (Original) The semiconductor integrated circuit of claim 7, further comprising an element isolation region disposed between said uniform base region and said drift region.